APPLICATION

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APPLICANT NAME: Terry C. Coughlin, Jr., et al.

TITLE: ASIC ARCHITECTURE FOR ACTIVE-COMPENSATION OF A PROGRAMMABLE IMPEDANCE I/O

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Name of person mailing paper Denise M. Jurik

Signature Denise M Jurik Date 2/7/2002

ASIC ARCHITECHTURE FOR ACTIVE-COMPENSATION OF A PROGRAMMABLE IMPEDANCE I/O

Background Of The Invention

Field of the Invention

This invention generally relates to I/O cells with programmable active input bias. More specifically, the invention relates to a circuit architecture, and to a method of using this circuit architecture, for an actively compensated and programmable impedance I/O.

Prior Art

CMOS I/O drivers require a tightly controlled driver impedance to maintain signal integrity when switched at high speeds. I/O drivers have been designed that maintain the driver's impedance by making adjustments for Integrated Circuit (IC) process variations, temperature and voltage changes. These I/O designs consist of a custom I/O circuit design and the overhead circuitry required to set the driver impedance for a given IC process; and then maintain this impedance when changes in temperature and voltage are sensed.

The design of such dynamically-controlled and programmable impedance drivers is often quite complex compared to I/O cell designs without this type of control. Custom circuit design, test, verification and characterization of the I/O can be quite time consuming and costly. For each additional technology offering, where these same controlled impedance I/O's are required, the lengthy design process must begin again.

Summary Of The Invention

An object of this invention is to improve circuits and methods for controlling the impedance of I/O drivers.
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Another object of the present invention is to provide a circuit architecture for an actively compensated and programmable impedance I/O.

A further object of the invention is to provide a circuit architecture, for controlling the impedance of I/O drivers, that can be translated to many technology offerings without redesigning the control circuitry.

Another object of this invention is to make the design time of a standard I/O equivalent to a dynamically controlled and programmable impedance I/O that was once only possible with a full custom circuit design.

These and other objectives are attained with a method of, and a circuit for, impedance control. The method comprises the steps of providing an input/output cell having a controllable input/output impedance, providing a reference cell including a node having a variable voltage, and comparing the voltage of the node to a reference voltage. The voltage of the node is adjusted during a defined period and according to a defined procedure, and during that defined period, a digital signal is generated. That digital signal is transmitted to the input/output cell to adjust the input/output impedance.

The preferred embodiment of the invention uses a circuit architecture for a circuit that provides an actively compensated and programmable impedance I/O that meets Application Specific Integrated Circuit (ASIC) methodology requirements and provides all the advantages of a custom circuit design. This architecture allows the design to be translated to any technology offering without redesigning the control circuitry. The main advantage the architecture provides is to make the design time of a standard I/O equivalent to a dynamically controlled and programmable impedance I/O that was once only possible with a full custom circuit design.

Further benefits and advantages of the invention will become apparent from a consideration of the following detailed description, given with reference to the

accompanying drawings, which specify and show preferred embodiments of the invention.

Brief Description Of The Drawings

Figure 1 shows a circuit architecture incorporating the invention.

Figure 2 is a block diagram of the system of Figure 1, showing all the input and output signal names.

Figure 3 shows the I/O cell of the architecture of Figure 1.

Figure 4 illustrates the driver impedance update logic for the I/O cell.

Figures 5 and 6 show the driver impedance update logic and truth table.

Figure 7 shows a receiver truth table.

Figure 8 illustrates the reference cell of the architecture of Figure 1.

Figure 9 is a reference cell truth table.

Figure 10 shows the relative timing of the control signals generated by the digital controller.

Detailed Description Of The Preferred Embodiments

Figure 1 shows a circuit architecture 10 generally comprising I/O cell 12 that is being controlled, reference cell 14, and digital controller 16. Figure 2 is a more detailed block diagram of architecture 10 showing all the input and output signal names.

The controller I/O cell 16, shown in detail in Figure 3, may be a typical high speed I/O with the addition of N number of control bits for pull-up and pull-down control of the driver Impedance. The I/O cell also has three additional control inputs PNDRIVE, NOUPDT and TESTUDT all of which come from the digital controller. A typical driver would pass data from an internal pin "A" and drive the data at the output pin "PAD" with a fixed driver impedance for both pull-up and pull-down. In the disclosed I/O cell, the driver impedance depends on the PFET control bits (PVTP[5:0]) and NFET control bits (PVTN[5:0]). The input "PNDRIVE" enables a default maximum value of driver impedance to be maintained. When all the control bit inputs are disabled, the output impedance will be at its maximum impedance level when PNDRIVE is enabled. When the controller enables additional input bits PVTP[5:0] and PVTN[5:0], the driver will switch on additional PFET and NFET fingers which will lower the output impedance and increase the drivers current strength. The control bits are binary weighted with bit "0" being the LSB and bit "5" being the MSB. This yields 32 bits of resolution for both the pull-up and pull-down impedance.

The input "NOUPDT" is a strobe input from the digital controller. When NOUPDT (no-update) is asserted, the I/O will not accept the control bit inputs PVTN[5:0] and PVTP[5:0]. The signal NOUPDT is asserted before the controller sends out new values of control bits and stays asserted until all the control bits are stable. This prevents glitching of the I/O impedance when the control bit values are changing. The input "TESTUPDT" is used during testing of the I/O. This input forces the I/O to propagate the values of the input control bits to the output driver during test.

Figure 4 Illustrates how the P/N - Bit Control Interface 20 operates in the controlled I/O cell. Figure 4 shows the logic for two PFET bits PVTP0 and PVTP5. The same logic is used for all bits PVTP[0:5] and PVTN[0:5]. Under normal operation, the input control bits are held in internal latches 22 and the PFET control bits are passed to the driver pull-up during a "one" to "zero" transition. Likewise, the NFET control bits are passed to the driver pull-down during a "zero" to "one" transition. This allows the digital controller to

operate at any speed (usually much slower), either synchronously or asnychronously from the high speed driver. The driver impedance update logic and truth table are shown in Figures 5 and 6.

The receiver is unaffected by the disclosed driver and operates as any prior art receiver circuit. The receiver truth table is shown in Figure 7.

The reference cell 14 is used to calibrate the driver impedance for all the controlled drivers on the chip. A block diagram of the reference cell is shown in Figure 8 and the truth table for this cell is shown in Figure 9. The driver impedance is set to match the impedance value of an external resistor 30 placed between nodes PADR and PADG. The reference cell is a physical copy of the driver output structure without the receiver and with some additional circuitry. The driver NFETs and PFETS in the I/O Cell are physically laid out as four parallel fingers that make up the total driver impedance. The calibration cell uses 1/4 of the driver NFETs and PFETs for calibration. By using 1/4 of the output stage, the external resistor becomes four times as large. When calibrating the driver impedance to 50 Ohms an external resistor of 200 Ohms is used.

There are two distinct advantages of using a calibration resistor that is four times larger. First, any pad transfer resistance difference between I/Os and any difference in line resistance between PADR and PADG is reduces by a factor of four. As an example, an additional 2 ohms of pad transfer resistance in a 50 ohm driver would be 2/50 or 4% error in driver impedance. This same 2 ohms compared to a 200 ohms calibration resistor is now 2/200 or 1%. The second advantage is the reduction in DC power of the calibration resistor by a factor of four. Using 1/4 of the output stage in the calibration cell also enables the calibration cell to be the same physical size as the driver, which is typically a requirement in an ASIC architecture.

The calibration cell functions as follows: An external resistor 30 placed between PADR and PADG acts as the pull-down NFETs of a driver set at a fixed impedance. The

digital controllers 16 sends a 6-bit binary count to the inputs CNTP[5:0]. If the count starts at 000000, the PFET pull-up tied to PADR are off and the voltage at PADR is compared to an internal reference voltage labeled Vddq/2. The comparator senses the voltage at PADR is less then the reference, and the output ZPCNTDWN goes low. The output ZPCNTDWN=0 tells the digital controller to increment the count at the inputs CNTP[5:0]. As the count increases, the relative strength of the pull-up PFETs increases and causes the voltage at PADR to increase. When the count reaches a point where the PFET pull-up impedance is greater than the reference voltage, the output ZPCNTDWN changes to a one. The digital controller will then reduce the count until ZPCNTDWN flips back to a zero.

When the digital controller senses the ZPCNTDWN signal is toggling between one and zero each count, a fixed count PVTP[5:0] is sent to the I/Os and calibration cell. The stable count PVTP[5:0] at the calibration cell is used to control a mirror copy of the PFETs controlled by CNTP[5:0]. The impedance of the PFETs controlled by PVTP[5:0] are equal to the external resistor and is used to calibrate the pull down NFET impedance. With a stable count at PVTP[5:0] the digital controller starts to increment the count at CNTN[5:0]. If CNTN[5:0] starts out at 000000, the pull-down NFETs are off and the voltage at VNEVAL is pulled to Vddq through the PFETs controlled by PVTP[5:0]. The output ZNCNTDWN = 0 is sent to the digital controller which forces the binary count at CNTN[5:0] to increment. CNTN[5:0] increases until the voltage at VNEVAL is greater than or equal to the internal reference Vddq/2.

At this point, the output ZNCNTDWN flips to a one. This NFET calibration works much the same way as the PFET calibration, where the controller will hold a stable count at CNTN[5:0] when it senses ZNCNTDWN is toggling each count. When a stable count is reached, the NFET impedance controlled by CNTN[5:0] matches the PFET impedance controlled by PVTP[5:0] which also matched the impedance of the external resistor. The counters will remain fixed until a change in temperature or voltage causes a change in impedance.

The EVAL is used to turn on all DC circuits in the calibration cell during an evaluation. This keep the DC power at zero when calibration is not required. The inputs SENSE and XFER are used by the comparators which are implemented as differential sense amplifiers. The signal SENSE nulls the comparator inputs to remove any offset. The signal XFER latches the comparator results each impedance evaluation cycle. The signal POR is a power on reset which puts the latched values of inputs PVTP[5:0], CNTN[5:0], CNTP[5:0] and outputs ZNCNTDWN and ZPCNTDWN in known states. The signals RI and ZRI are used for testing.

The digital controller is an ASIC synthesizable logic macro that provides the control signals for the controlled and reference I/O cells. The logical design of the digital controller is fairly compact and simple; this lends to the controller's technology-independent nature, and thus it can be synthesized using primitive and basic logic blocks commonly found in most technology cell libraries. This allows the design to be translated to any technology offering without redesigning the control circuitry, hence dramatically reducing the design time of the programmable impedance I/O scheme.

The digital controller generates and applies the proper circuit bias signals to the calibration/reference cell, increments or decrements the impedance control value as necessary, and outputs the resultant stable impedance value to the I/O cells. The digital controller contains a 6-bit incrementer which is clocked by CLK. The incrementer resets whenever POR (power-on-reset) is active or when ENABLE is inactive. The incrementer can be viewed as a system clock cycle counter which determines the proper timing of the I/O and calibration cell control signals. A complete impedance evaluation cycle is considered to have occurred if the cycle counter has counted from b000000 to b111111 without being interrupted by POR or ENABLE. In other words, the impedance evaluation cycle is equivalent to 64 system CLK cycles. The relative timing of the control signals generated by the digital controller is shown in Figure 10.

ZEVAL is used to turn on all DC circuits in the calibration cell during an impedance evaluation; hence it keeps the DC power at zero when calibration is not required. ZSENSE and ZXFER are used by the comparators located in the calibration cell which are implemented as differential sense amplifiers. ZSENSE nulls the comparator inputs to remove any offsets. ZXFER latches the comparator results each impedance evaluation cycle.

ZCNTN[5:0] and ZCNTP[5:0] are the latched impedance control values sent to the calibration cell for evaluation with the reference values. ZPVTN[5:0] and ZPVTP[5:0] are the latched impedance control values sent to the I/O cells. In general, the impedance values ZPVTx will only update after two consecutive and identical evaluations of ZCNTx are detected (ie, two consecutive evaluation cycles with xCNTDWN = '1' or two consecutive evaluation cycles with xCNTDWN = '0'). When this occurs, the impedance values will update in the evaluation cycle immediately following these two identical evaluation cycles. This behavior ensures the output of a "stable" ZPVTx impedance value when the voltage comparator is oscillating between latching a '1' and latching a '0' in xCNTDWN during consecutive evaluation cycles, indicating that the proper impedance level has been reached. The only exception to this rule is when ZCNTx maintains the same value for two consecutive evaluation cycles, in which case only one evaluation cycle with xCNTDWN=0 is required before ZCNTx is increased. This scenario arises upon POR completion, or when both ZCNTx and ZPVTx reach their minimal values.

It may be noted that the evaluation of ZCNTN is based upon the previous evaluation of ZPVTP; ZPVTP controls the "mirrored" PFET evaluation stack. This means ZPVTN in any given evaluation cycle is based upon the ZPVTP of the previous evaluation cycle.

CLKA, CLKB, and CLKC are the standard ASIC LSSD test clock signals. SI is the LSSD scan chain input, and ZSO is the LSSD scan chain output. In addition to these standard LSSD test signals, the digital controller also has a special signal ZPNDRIVE

that facilitates testing of the I/O cells in the case when all of the impedance control bits are disabled. ZPNDRIVE enables the default NFET and PFET driver fingers, so that the driver will not be completely shut off in this case.

The preferred embodiment of the digital controller, as described in detail, is designed as a synthesized core or macro. The advantage of this implementation is that it never has to be redesigned in future technologies. The digital controller is carried over to future technologies in the form of VHDL code, which is pure logic and independent of technology. This is one feature that separate this ASIC architecture from a full custom design. This method provides an important advantage over prior art.

While it is apparent that the invention herein disclosed is well calculated to fulfill the objects previously stated, it will be appreciated that numerous modifications and embodiments may be devised by those skilled in the art, and it is intended that the appended claims cover all such modifications and embodiments as fall within the true spirit and scope of the present invention.